

P50LF10SLK

Power MOSFETs

100V, 50A, N-channel

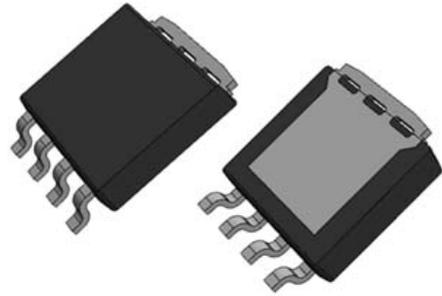
Feature

- N-channel
- Small SMD
- Large Current
- Low Ron
- 4.5V Gate Drive
- Low Capacitance
- Based on AEC-Q101
- Halogen free
- Pb free terminal
- RoHS:Yes

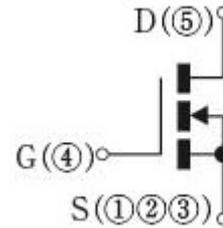
OUTLINE

Package (House Name): LF

Package (JEDEC Code): MO-235B similar



Equivalent circuit



Absolute Maximum Ratings (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	Tstg		-55 to 175	°C
Channel temperature	Tch		-55 to 175	°C
Drain-source voltage	V _{DSS}		100	V
Gate-source voltage	V _{GSS}		±20	V
Continuous drain current(DC)	I _D		50	A
Continuous drain current(Peak)	I _{DP}	Pulse width 10μs, duty=1/100	200	A
Total power dissipation	P _T		217	W
Single avalanche current	I _{AS}	Starting T _{ch} =25°C T _{ch} ≤150°C	35	A
Single avalanche energy	E _{AS}	Starting T _{ch} =25°C T _{ch} ≤150°C	140	mJ

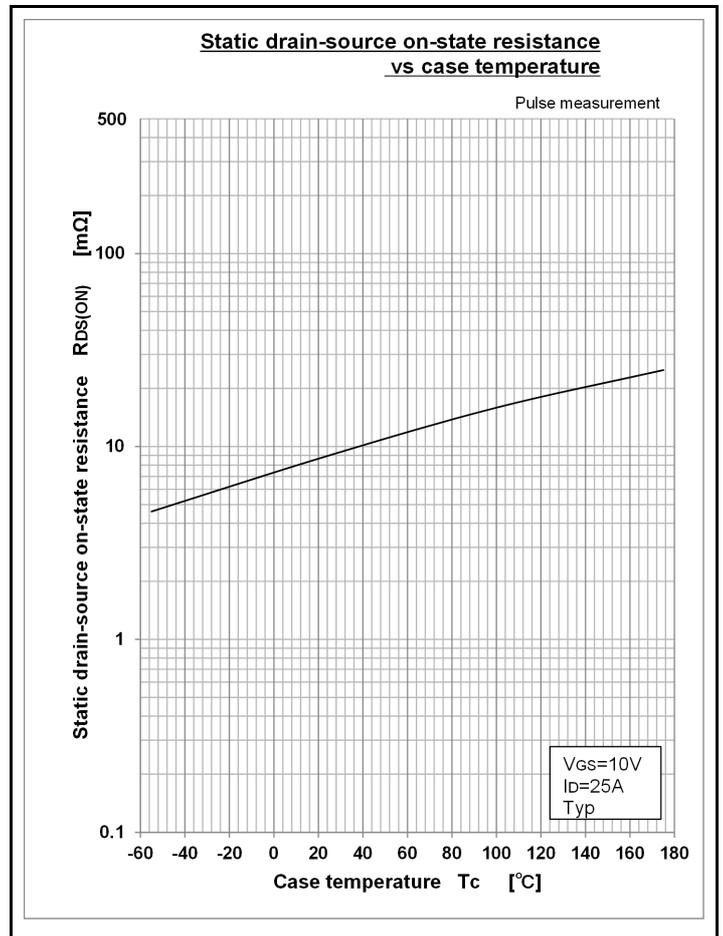
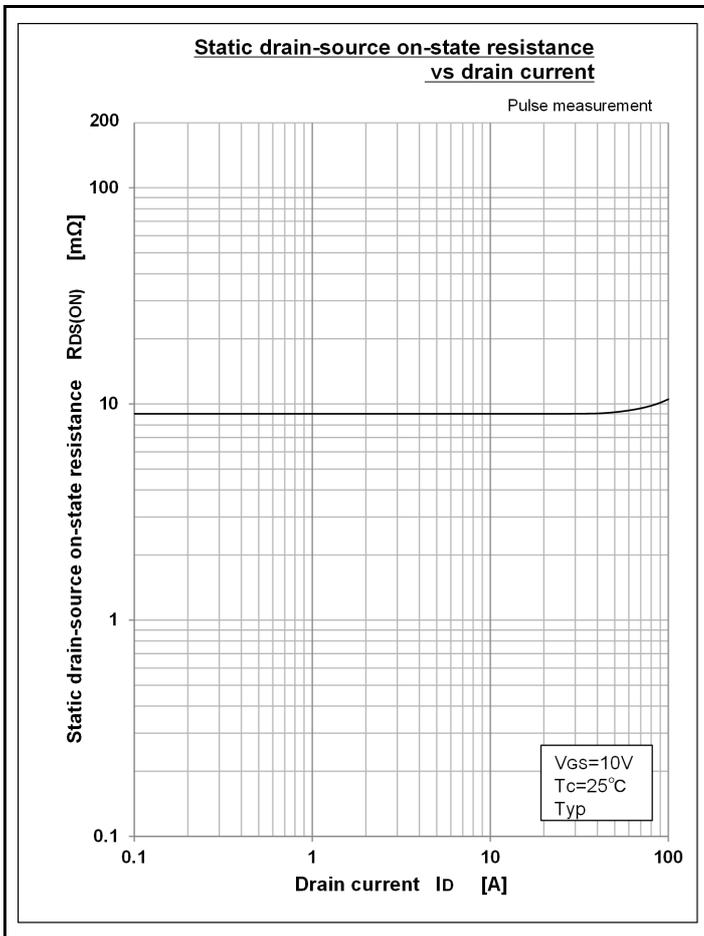
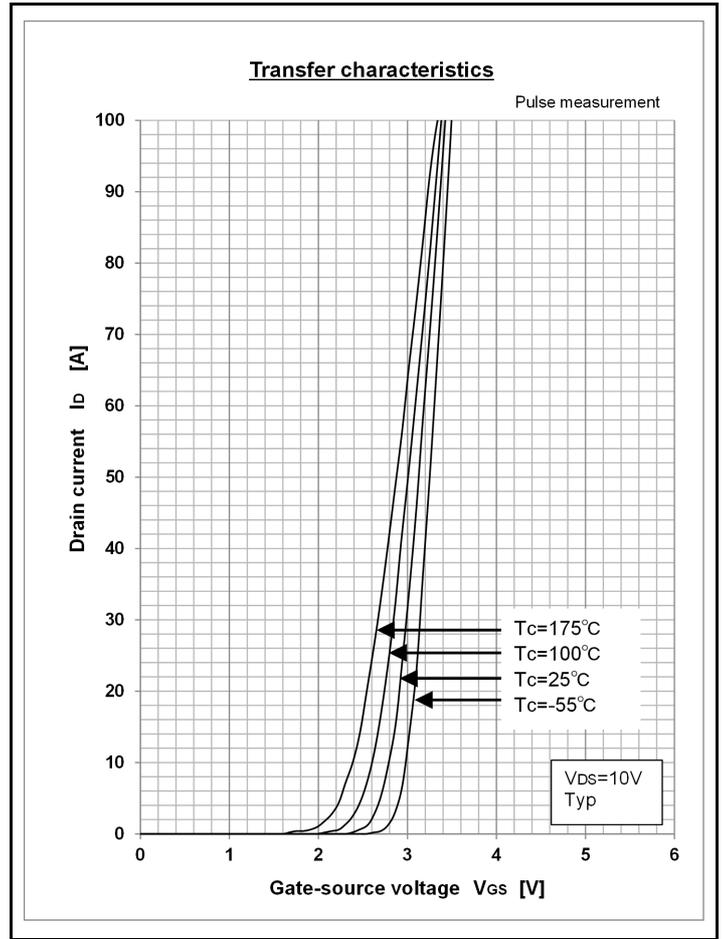
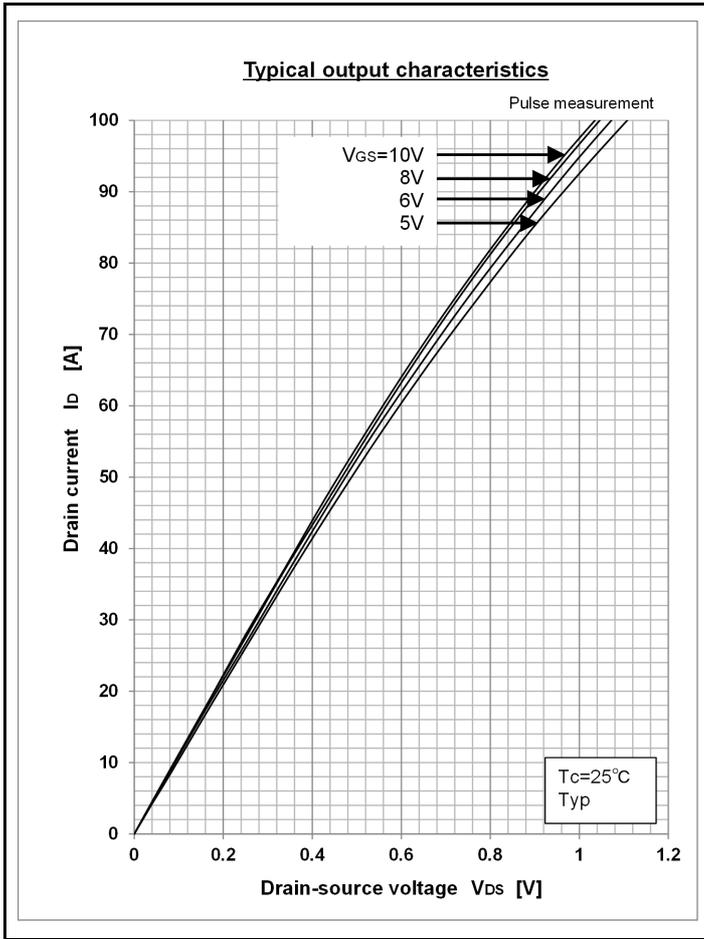
* : See the original Specifications

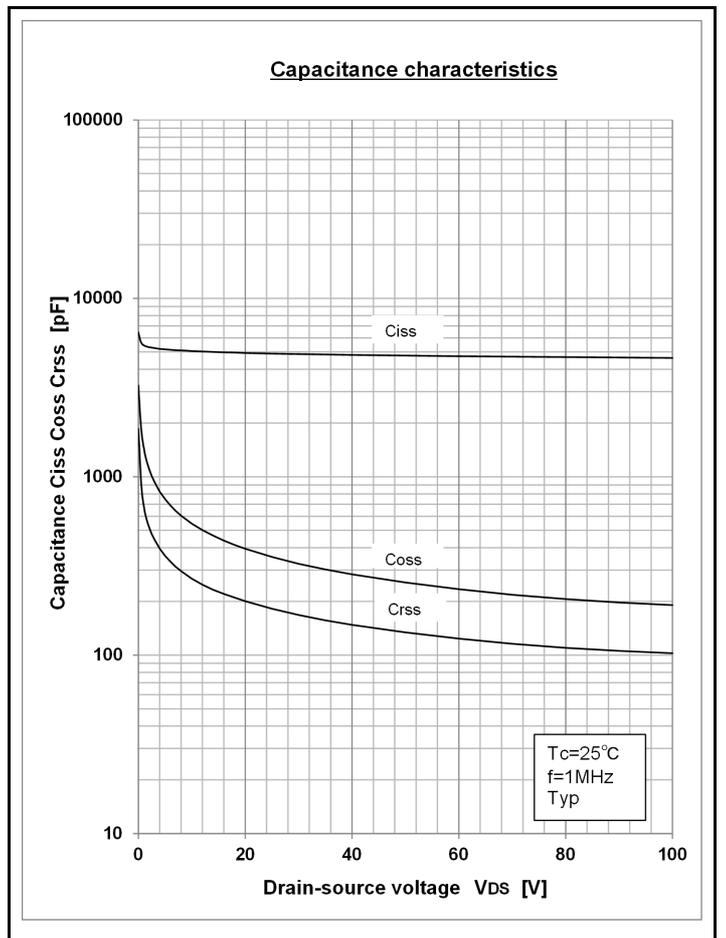
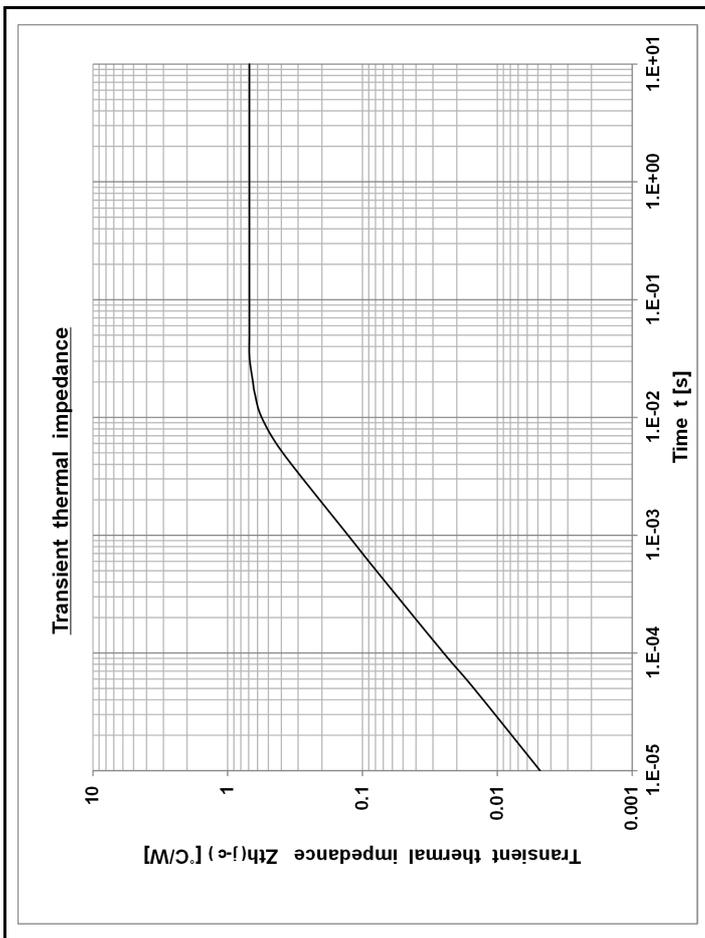
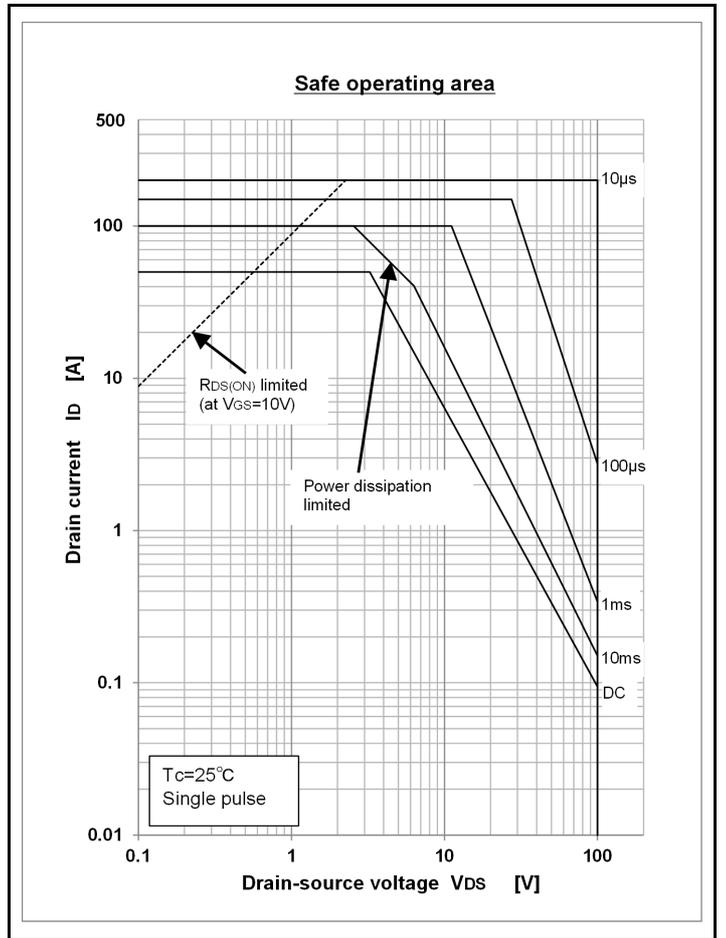
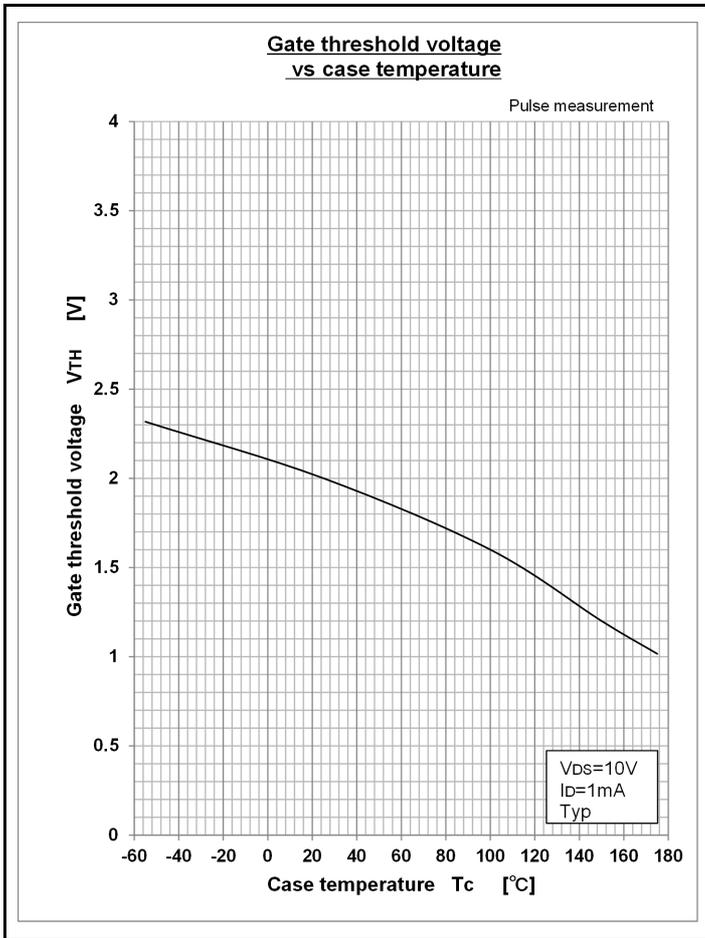
Electrical Characteristics (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	ID=1mA, VGS=0V	100			V
Zero gate voltage drain current	I_{DSS}	VDS=100V, VGS=0V			1	μA
Gate-source leakage current	I_{GSS}	VGS=±20V, VDS=0V			±0.1	μA
Forward transconductance	g_{fs}	ID=25A, VDS=10V	20			S
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=25A, VGS=10V		0.009	0.0113	Ω
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=25A, VGS=4.5V		0.0099	0.0132	Ω
Gate threshold voltage	V_{th}	ID=1mA, VDS=10V	1.5	2	2.5	V
Source-drain diode forward voltage	V_{SD}	IS=50A, VGS=0V			1.5	V
Thermal resistance	$R_{th(j-c)}$	Junction to case, with heatsink			0.69	°C/W
Total gate charge	Q_g	VDD=80V, VGS=10V, ID=50A		102		nC
Gate to source charge	Q_{gs}	VDD=80V, VGS=10V, ID=50A		18		nC
Gate to drain charge	Q_{gd}	VDD=80V, VGS=10V, ID=50A		28		nC
Input capacitance	C_{iss}	VDS=25V, VGS=0V, f=1MHz		4900		pF
Reverse transfer capacitance	C_{rss}	VDS=25V, VGS=0V, f=1MHz		182		pF
Output capacitance	C_{oss}	VDS=25V, VGS=0V, f=1MHz		355		pF
Turn-on delay time	$t_{d(on)}$	ID=25A, RL=2.00Ω, VDD=50V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		6		ns
Rise time	t_r	ID=25A, RL=2.00Ω, VDD=50V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		11		ns
Turn-off delay time	$t_{d(off)}$	ID=25A, RL=2.00Ω, VDD=50V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		102		ns
Fall time	t_f	ID=25A, RL=2.00Ω, VDD=50V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		32		ns
Diode reverse recovery time	t_{rr}	IF=50A, VGS=0V, di/dt=100A/μs		58		ns
Diode reverse recovery charge	Q_{rr}	IF=50A, VGS=0V, di/dt=100A/μs		128		nC

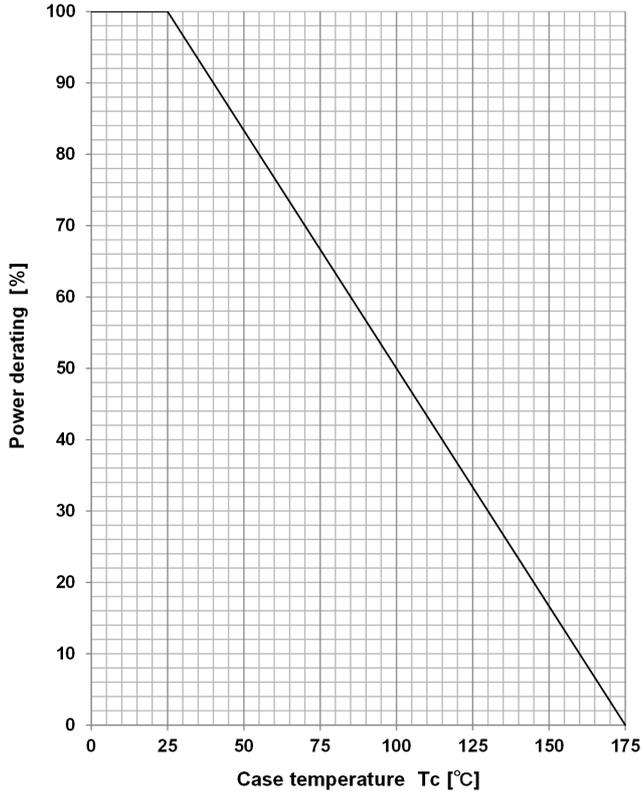
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CHARACTERISTIC DIAGRAMS

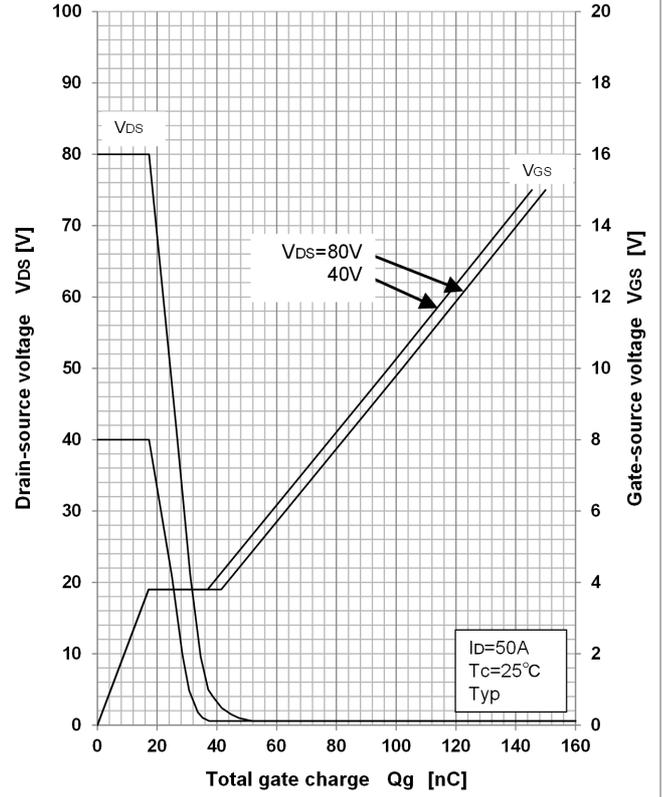




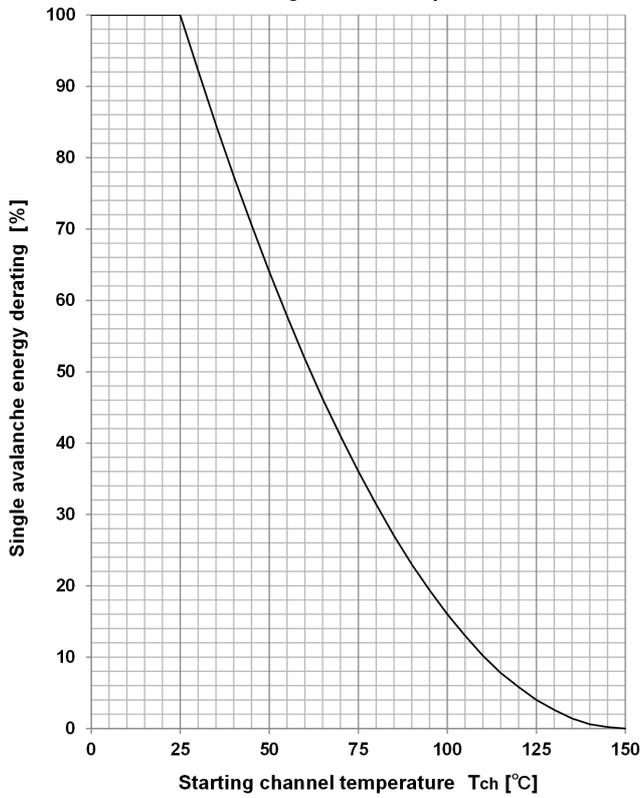
Power derating vs case temperature



Gate charge characteristics

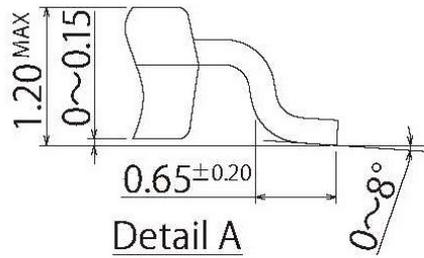
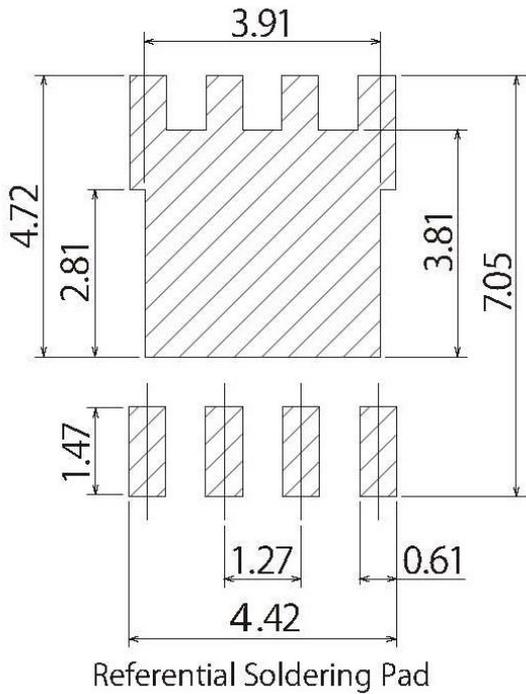
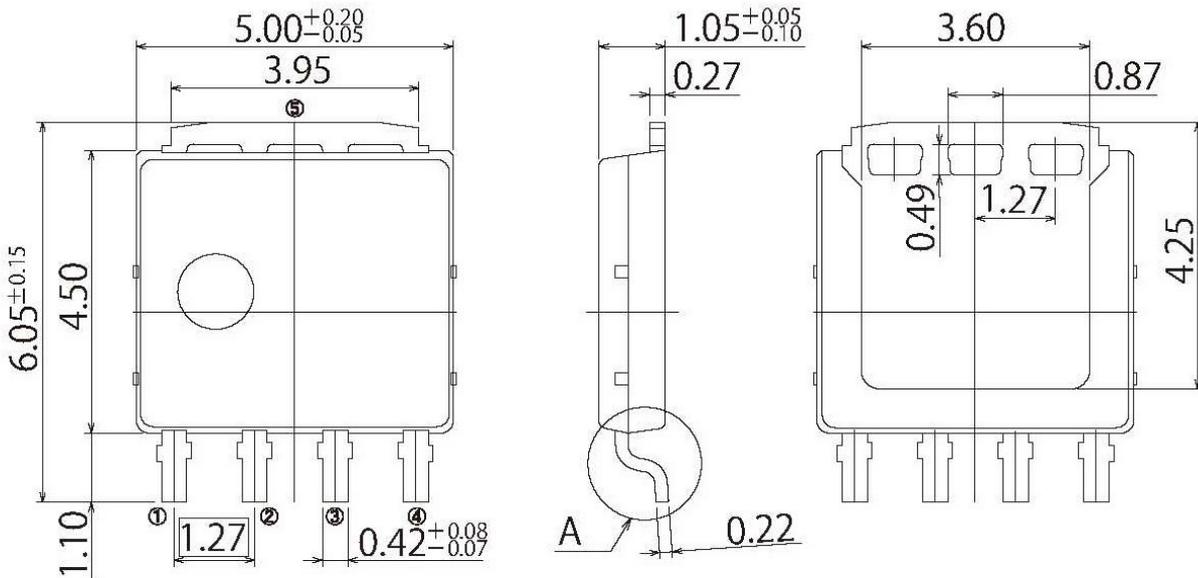


Single avalanche energy derating vs starting channel temperature



G7

JEDEC Code	MO-235B similar
JEITA Code	—
House Name	LF



• Optimize soldering pad to the board design and soldering condition.

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